AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A system comprising:

a clock for generating a clock signal at half a rate of transmitted serial data from a signal source;

a half-rate phase detector coupled to the clock and the signal source for oversampling the transmitted serial data and providing sampled data, and for detecting and grouping phase transitions between a phase lead and a phase lag in the sampled data and outputting phase transition data;

a phase selector;

an encoder, coupled to the half-rate phase detector, for encoding the phase transition data according to an optimum phase selected by the phase selector; and

a confidence counter coupled to the encoder to receive the encoded phase transition data and provide an output representative of an accumulated effect of the phase transitions~~; and~~ based on the encoded phase transition data,

wherein the [[a]] phase selector[[,]] is coupled to receive the clock signal and the output from the confidence counter~~, for selecting an~~ to select the optimum phase effective for recovering the clock relative to the transmitted serial data.

2. (Original) The system of claim 1, wherein the phase detector oversamples the transmitted serial data at four times the half rate of the transmitted serial data.

3. (Original) The system of claim 1, wherein the clock signal has eight phases for each period in the transmitted serial data.

4. (Original) The system of claim 1, wherein the clock comprises a delay locked loop.

5. (Original) The system of claim 1, wherein the clock comprises a phase locked loop.

6. (Original) The system of claim 1, wherein the confidence counter comprises a state machine for identifying each of the detected phase leads and the detected phase lags.

7. (Original) The system of claim 6, wherein the state machine further comprises an initial state, eight states for each detection of the phase lead, and eight states for each detection of the phase lag.

8. (Original) The system of claim 1, wherein the phase selector comprises a state machine having four states for shifting the sampling phase toward the optimum phase.

9. (Original) The system of claim 1, wherein the phase detector performs XOR logic operations.

10. (Original) The system of claim 1 further comprising a multiplexer coupled to receive the recovered clock and the oversampled data and output the transmitted data.

11. (Currently Amended) A clock and data recovery method comprising:

generating a clock signal at half a rate of transmitted serial data;

oversampling the transmitted serial data and providing sampled data;

detecting and grouping phase transitions between a phase lead and a phase lag in the sampled data and outputting phase transition data;

encoding the phase transition data according to an optimum phase selected by a phase selector;

providing an output representative of an accumulated effect of the encoded phase transitions based on the encoded phase transition data; and

selecting [[an]] the optimum phase effective for recovering the clock relative to the transmitted serial data.

12. (Original) The method of claim 11 further comprising oversampling the transmitted serial data at four times the half rate with respect to the clock signal for each period of the transmitted serial data.

13. (Original) The method of claim 11, wherein the clock signal comprises eight phases.

14. (Original) The method of claim 11 further comprising multiplexing the recovered clock and the oversampled data for outputting the transmitted serial data.

15. (Original) The method of claim 11 further comprising performing logic operations in selecting the optimum phase.

16. (Original) A system comprising:

a clock for generating an 8-phase clock signal at half rate of transmitted serial data;

a half-rate phase detector for oversampling the transmitted serial data at four times the half clock rate and providing sampled data, and for detecting and grouping phase transitions between a phase lead and a phase lag in the sampled data and outputting phase transition data;

a phase selector;

an encoder encoding the phase transition data according to an optimum phase selected by the phase selector; and

a confidence counter coupled to receive the encoded phase transition data and provide an output representative of an accumulated effect of the phase transitions~~; and,~~

wherein the [[a]] phase selector[[,]] is coupled to receive the clock signal and the output from the confidence counter~~, for selecting an~~ to select the optimum phase effective for recovering the clock relative to the transmitted serial data.

17. (Original) The system of claim 16, wherein the confidence counter comprises a state machine for identifying each of the detected phase leads and the detected phase lags.

18. (Original) The system of claim 17, wherein the state machine further comprises an initial state, eight states for each detection of the phase lead, and eight states for each detection of the phase lag.

19. (Original) The system of claim 16, wherein the phase selector comprises a state machine having four states for shifting the sampling phase toward the optimum phase.

20. (Original) The system of claim 16 further comprising a multiplexer coupled to receive the recovered clock and the oversampled data and output the transmitted data.

21. (New) The system of claim 9, wherein input data in the XOR logic gate have a phase transition rate twice of phase resolution of the phase detector.

22. (New) The system of claim 9, wherein XOR logic operation results are grouped into two sets according to sampled clock phases.

23. (New) The system of claim 9, wherein the encoder encodes output data of the phase detector according to the optimum phase of the phase selector.